ABSTRACT OF THE DISCLOSURE

Two common varieties of test interfaces exist for ICs and/or cores, the IEEE 1149.1 Test Access Port (TAP) interface and internal scan test ports. The TAP serves as a serial communication port for accessing a variety of circuitry including; IEEE 1149.1 boundary scan circuitry, built in self test circuitry, internal scan circuitry, IEEE 1149.4 mixed signal test circuitry, IEEE P5001 in-circuit emulation/debug circuitry, and IEEE P1532 in-system programming circuitry. Internal scan test ports serve as a serial communication port for primarily accessing internal scan circuitry within ICs and cores. Today, the TAP and internal scan test ports are typically viewed as being separate test interfaces, each utilizing different IC pins and/or core terminals. The need for different IC pins and/or core terminals is overcome by an interface in accordance with the invention that allows the TAP and internal scan test ports to be merged so they both can co-exist and operate from the same set of IC pins and/or core terminals. Further, this interface allows merged TAP and scan test port interfaces to be selected individually or in groups.